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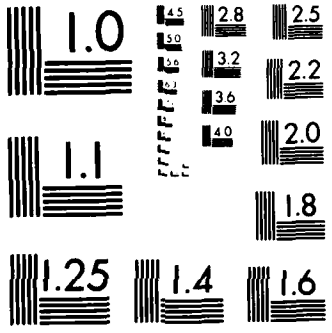
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Center for Integrated Electronics
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COMPLETELY CONSUMED CARBIDE (C^3) - A NEW PROCESS FOR DIELECTRIC ISOLATION

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ABSTRACT

A new process for dielectric isolation based on the use of silicon carbide has been investigated. This process uses the lower oxidation rate of SiC compared to Si to provide local regions of thick field oxide. If the local oxidation process results in the complete consumption of the carbide (C^3) film, then a high quality MOS structure is obtained. In this paper, this C^3 process is compared to the standard silicon nitride LOCOS process. MOS capacitors and Schottky barrier diodes have been fabricated with both techniques for varying pad oxide thickness (0,100,200Å). The effect of high temperature anneal on these structures has been investigated. The electrical properties of these devices have been measured. This includes lifetime, breakdown voltage and I-V characteristics. For the minimum bird's beak case (no pad oxide) the C^3 process results in superior electrical properties over the standard nitride process.

I. INTRODUCTION

Recently, the oxidation properties of silicon carbide thin films have been reported [1,2]. Since the oxidation rate of SiC was found to be considerably lower than that of Si, the feasibility of using SiC for a local oxidation process was investigated. In order to make the study more meaningful, the carbide process was compared to the standard silicon nitride LOCOS process [3,4] wherever possible.

II. EXPERIMENTAL PROCEDURE

To investigate the resulting electrical properties of

devices fabricated with a carbide-base dielectric isolation process, two types of structures were used: MOS capacitors and Schottky barrier diodes. Figure 1 indicates the process flow for both the carbide- and nitride-based processes. For the MOS capacitors 8-15 Ω-cm p-type Si wafers were used, while for the Schottky diodes 3-5 Ω-cm n-type wafers were used. The MOS capacitor had an area of 500 x 800μm^2 and the Schottky diodes had a circular area of $1.3 \times 10^{-3} cm^2$. To minimize stress and resulting damage, a thin oxide pad is normally used under the nitride layer in the conventional LOCOS process. However, this results in the undesirable feature of a larger "bird's beak" [4]. Therefore, in the experiments reported here, structures with and without an oxide pad were fabricated and compared. The pad oxidation was performed at 950°C in dry O_2 for either 10 min (~ 100Å) or 34 min (~ 200Å). For the carbide process, SiC was then deposited by RF sputtering in Ar from a hot-pressed stoichiometric composite target at 300°C. Typical SiC film thickness was around 900Å. All carbide films were annealed in H_2 at 1100°C to improve their oxidation resistance. For the nitride-based process, Si_3N_4 films of approximately the same thicknesses were deposited by CVD from the reaction of NH_3 and SiH_4 at 950°C. While the nitride films do not normally require to be annealed after deposition, this step was included for some of the samples in order to have a meaningful comparison with the corresponding carbide samples. All samples were then patterned using plasma etch with CF_4/4% O_2 at a pressure of 300 m Torr. Following the patterning of the carbide or nitride layer field oxidation was performed in wet O_2 at 950°C for 8 hours resulting in a field oxide thickness of approximately 8500Å. Under oxidation conditions, the complete consumption of the carbide layer results, hence the C^3 process. In its place a 4000Å SiO_2 layer is present. For the C^3 process, this oxide is etched back in HF resulting in a field oxide of 4500Å. In the nitride process, the nitride is first removed in hot H_3PO_4 followed by the removal of the pad oxide (if present) in HF. From this point on the two processes are identical. To fabricate the MOS capacitors, the following process steps are used:

a. Gate oxidation at 1050°C in dry O_2 for 30 minutes resulting in 500Å of SiO_2; then annealing in N_2 for 30 minutes.
b. Al deposition, ~ 8000Å.
c. Al patterning (wet etch).
d. Al sintering at 450°C for 20 minutes in N_2/H_2 (90/10).

For the Schottky diodes, a similar process was used except that no gate oxidation and no Al sintering were

used. In addition, in order to provide ohmic contact to the Si substrate, the backside of the samples was implanted with phosphorus at a dose of $2 \times 10^{15}/cm^2$ and an energy of 100 KeV.

The damage at the Si surface resulting from the two processes was first qualitatively studied using a Secco etch [5]. The surface morphology of the decorated Si surfaces for the samples fabricated without pad oxide is shown in Figure 2. For the C^3 process, a uniform distribution of damage sites is observed in Figure 2a. The damage sites are probably due to the deposition method (sputtering) used, in that Ar incorporated in the film during deposition can subsequently result in voids. On the other hand, for the conventional process a heavy distribution is observed at the periphery of the nitride region, Figure 2b. This clustering at the edge of the nitride mask (shown at higher magnification in Figure 2c) is probably due to the very low oxidation rate of the nitride and the consequently high stress present at the mask edge. Occasional damage sites are also seen within the mask region.

III. ELECTRICAL PROPERTIES

Electrical properties of the MOS capacitors and Schottky barrier devices implemented with both processes were measured.

(a) MOS Capacitors

For the MOS capacitors, C-V profiles and C-t measurements were performed to obtain threshold voltage, lifetime, surface recombination velocity and other parameters. In the absence of the pad oxide, the generation lifetime of the C^3-processed samples averaged 0.9μsec (over 20 samples) with a range from 0.04 to 4.2μsec. For the corresponding nitride case, the average lifetime (over 17 samples) was found to be 0.073μsec with a range from 0.026 to 0.13μsec. Similarly, the surface recombination velocity (S_0), as determined from Zerbst analysis, also indicated a better Si/SiO_2 interface for the C^3 process. Specifically, the average S_0 was 36 cm/sec for the C^3 samples, as compared to an average of 91 cm/sec for the conventional nitride process. Surprisingly, the surface properties of C^3 samples did not improve with the introduction of pad oxides as thick as 200Å. When the nitride samples are subjected to the same annealing cycle as the carbide samples, early breakdown prevents an accurate measurement of the lifetime, with and without pad oxide. The threshold voltage did not vary greatly (- 0.4 to - 0.8V) between the two processes with or without pad oxide.

Another important electrical parameter for MOS capacitors is the oxide breakdown voltage. Figure 3 shows a matrix of breakdown field histograms for the two processes. Without pad oxide, the C^3 process yields a higher breakdown field (averaging 2.8 MV/cm) than the conventional process (which averages 1.6 MV/cm). Indeed, if one anneals the nitride samples the average breakdown field is further reduced to 0.85 MV/cm. The addition of pad oxide significantly improves the breakdown field for the C^3 samples and for the standard process, reaching 6.1 and 6.9 MV/cm, respectively, with a 200Å pad oxide. Only in the case of the annealed nitride samples, does the pad oxide result in no improvement.

(b) Schottky Barrier Diodes

To further comparatively examine the surface properties of samples fabricated with C^3 and conventional nitride processes, aluminum barrier Schottky diode characteristics on n-type silicon wafers were measured. Figure 4 shows forward I-V characteristics of four different samples: Sample M is the control wafer on virgin silicon, Sample A is a C^3 sample, and Samples B and C are the nitride samples without and with the 1100°C anneal cycle. No pad oxide was used on all samples. It is clear that the C^3 sample resembles strongly that of the control sample in having a Schottky barrier height of 0.69 eV and an ideality factor of 1.1, similar to those reported in the literature [6]. On the other hand, the nitride samples, even before the high-temperature anneal have much poorer I-V characteristics, indicating a higher degree of surface damage. After the anneal, the nitride samples degrade further. With reverse bias applied, the same trend applies - with control and C^3 samples having the lowest leakage and the nitride sample after anneal having the highest.

As far as the Schottky characteristics are concerned, the samples fabricated with the C^3 process with a 100 to 200Å of pad oxide also show better forward and reverse behavior than the samples fabricated with the nitride process.

IV. SUMMARY

Comparing the new C^3 process with the conventional nitride LOCOS process, it was found that without pad oxide the former is superior in having more uniform and possibly lower damage distribution as shown in the SEM photographs. The better surface properties obtained in the C^3 process are confirmed by MOS and Schottky diodes measurements. Specifically, an improvement in lifetime, breakdown field,

and forward and reverse Schottky characteristics have been measured. In conclusion, it appears that the C^3 process is a promising technique for dielectric isolation of integrated circuits.

Two of the authors (W.-J. Lu and A.J. Steckl) would like to acknowledge partial support from the Office of Naval Research.

V. REFERENCES

[1] W.-J. Lu, T.P. Chow, A.J. Steckl and W. Katz "Thermal Oxidation of Sputtered Silicon Carbide Thin Films". J. Electrochem. Soc., 131, 1907 (1984) and ECS Extended Abstracts, 83-1, 133 (May 1983).

[2] C.D. Fung and J.J. Kopanski "Thermal Oxidation of 3C Silicon Carbide Single - Crystal Layers on Silicon". Appl. Phys. Lett., 45, No. 7, 757 (1984).

[3] J.A. Appels, E. Kooi, M.M. Paffen, J.J.H. Schatorje and W.H.C.G. Verkuylen "Local Oxidation of Silicon and Its Application in Semiconductor - Device Technology". Philips Res. Repts., 25, 118 (1970).

[4] W.G. Oldham "Isolation Technology for Scaled VLSI". IDEM Technical Digest 82, IEEE Conf. No. 82CH1832-5, p. 216 (December 1982).

[5] F. Secco d'Aragona "Dislocation Etch for (100) Planes in Silicon". J. Electrochem. Soc., 119, 948 (1972).

[6] A.Y.C. Yu and C.A. Mead "Characteristics of Aluminum-Silicon Schottky Barrier Diode"., Solid-State Electronics, 13, 97 (1970).

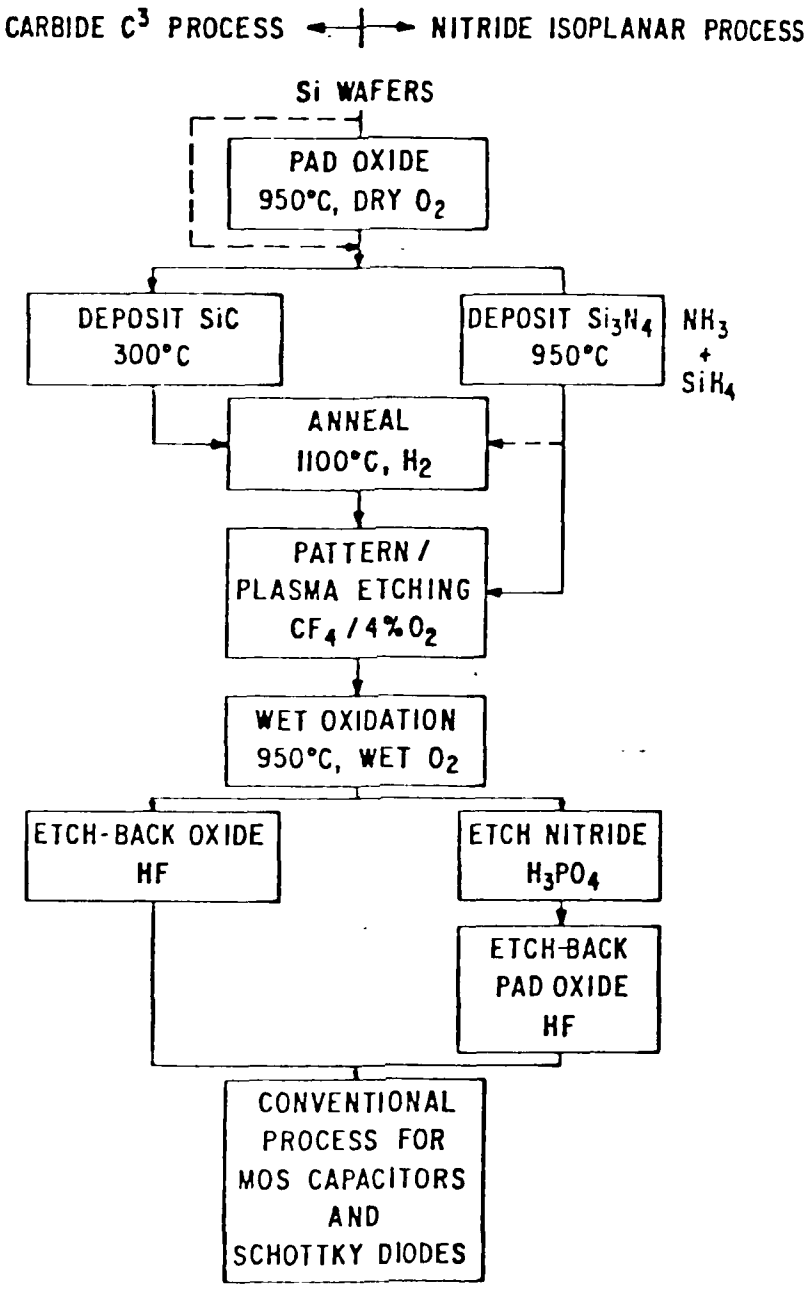
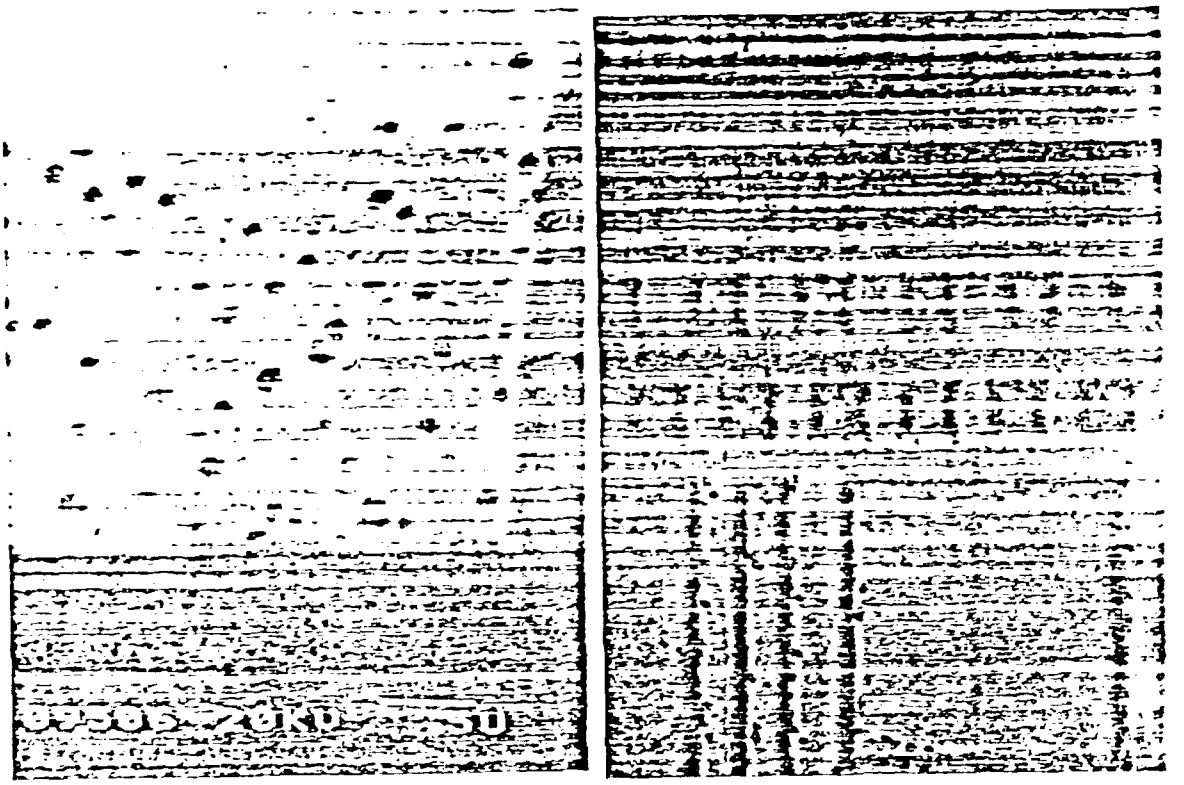
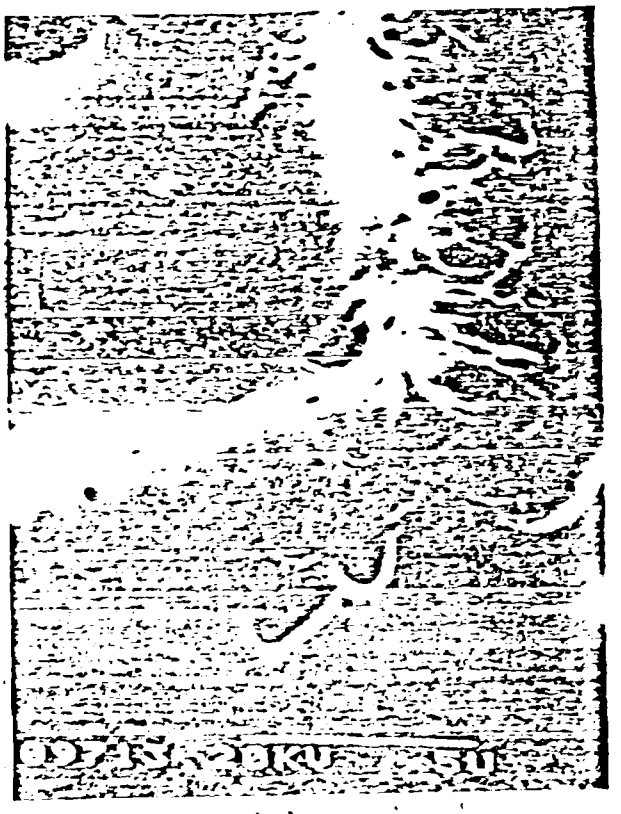


Fig. 1 Process flow diagram for both the carbide- and nitride-based processes.



(a) (b)



(c)

Fig. 2 Surface morphology of the decorated Si surface by Secco etch:
(a) C^3 process sample.
(b) Nitride process sample.
(c) Higher magnification of (b)

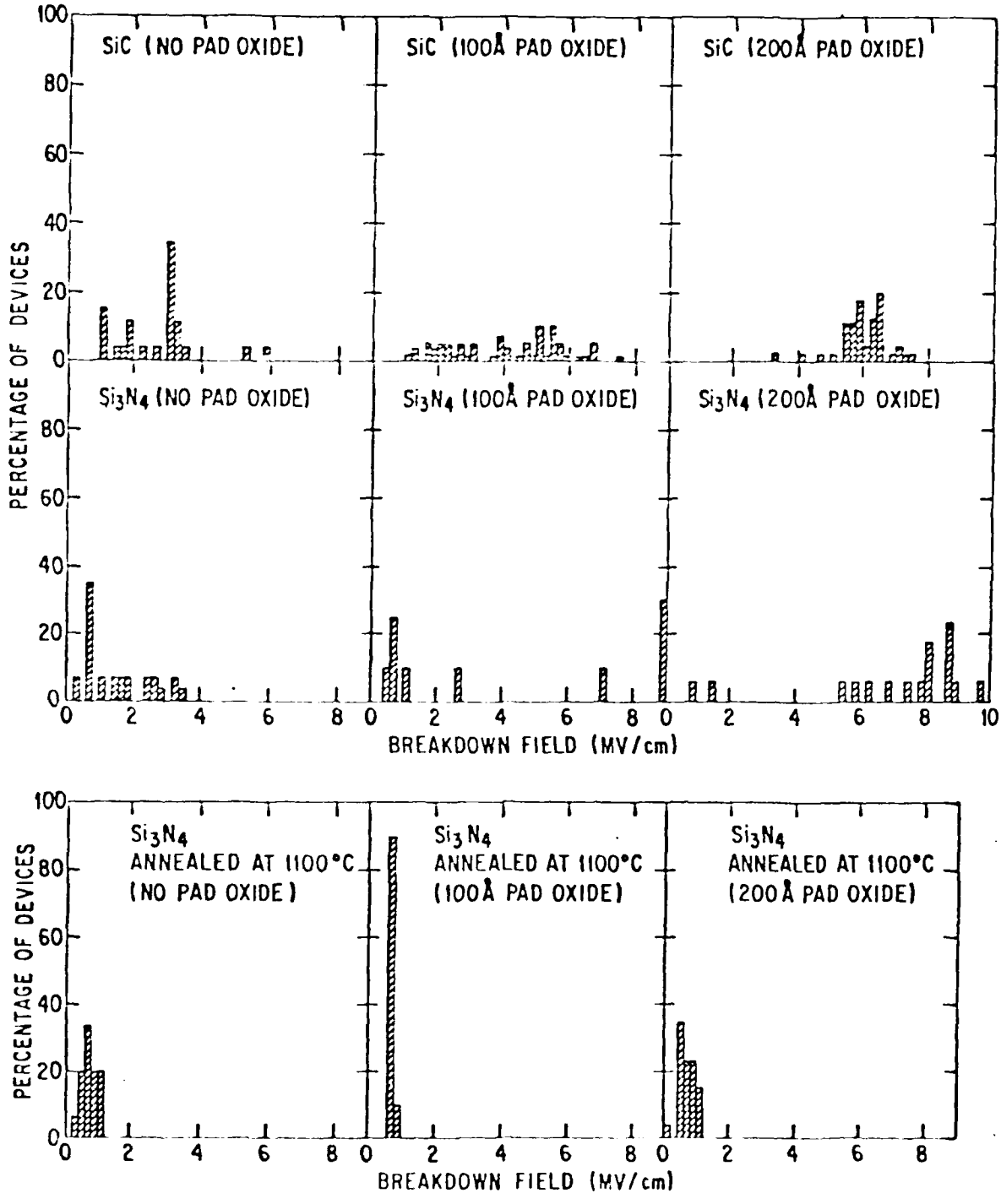


Fig. 3 MOS capacitor breakdown field histograms for carbide- and nitride-based processes with various pad oxide thickness.

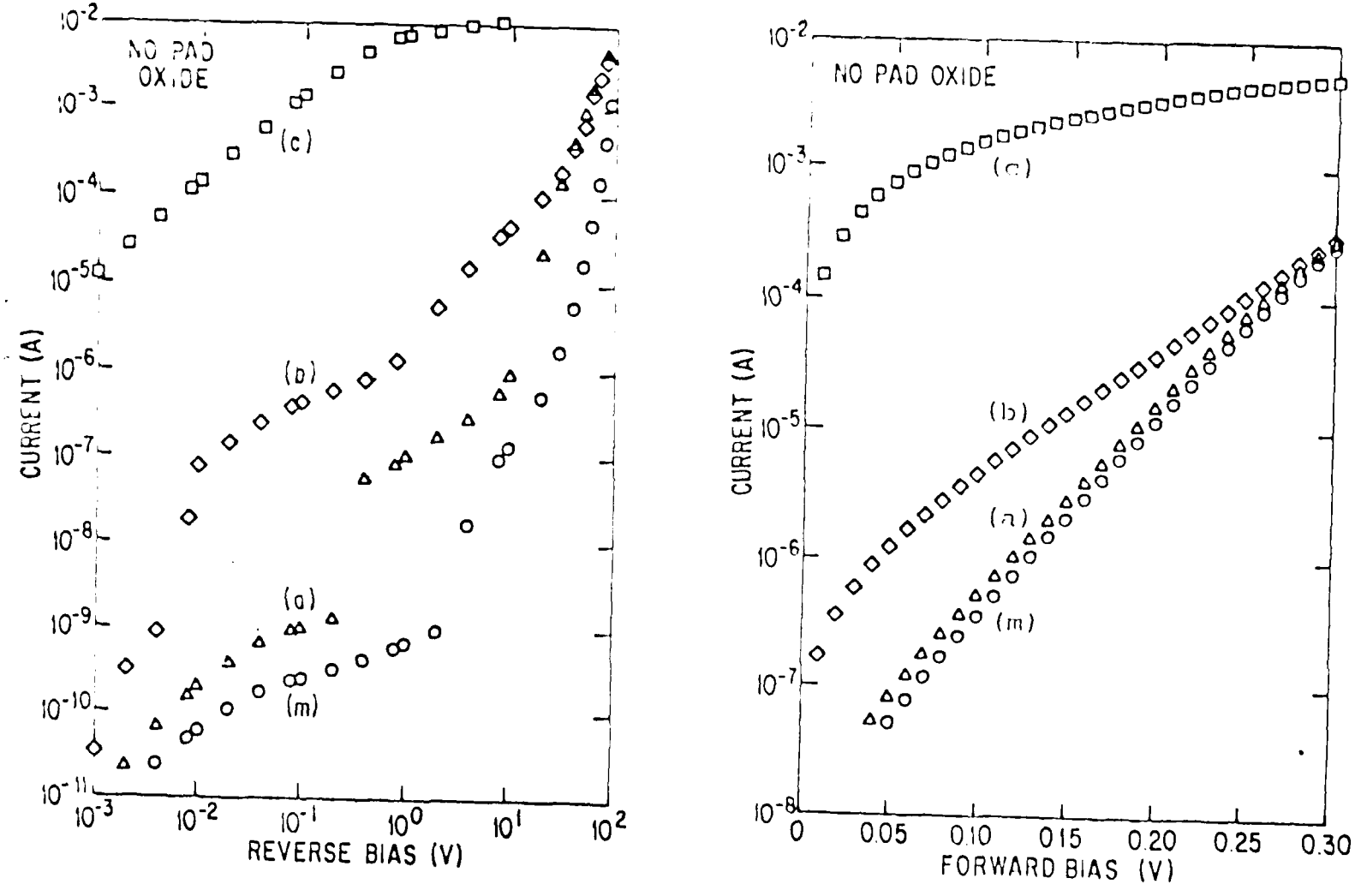


Fig. 4 I-V characteristics of Al-Si Schottky diodes fabricated by both processes.

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